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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/587,604
Filing Date: July 27, 2006
Appellant(s): DE GREEF, PETRUS MARIA

Terry W. Kramer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 14 August 2009 appealing from the Office action mailed 11 June 2009**(2) Related Appeals and Interferences**

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

Appeal Brief Filed March 18, 2009.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

EP 0 875 882 A22	Schiefer et al.	04-1998
European Patent Application Publication		
2003/0164897	Chen et al.	09-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, already of record, hereafter, '882).

Regarding claim 1, Schiefer teaches a display method comprising: generating images comprising source data (input video; '882; fig. 1 & 2; col. 10, ln. 14-26) and source frame (vertical) synchronization instants (IPVSYNC) having a source frame rate, storing the source data in a frame memory (memory, '882; fig. 3; col. 11, ln. 51-58; col. 18, ln. 13-39) under control of a first address pointer (write counter) having a start address being determined by the source frame synchronization instants (IPVSYNC) ('882; col. 13, ln. 13-39), reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants (DVSYNC) having a display frame

rate ('882; col. 14, ln. 5-35), displaying the display data on a matrix display ('882; fig. 2) and controlling the source frame rate or the display frame rate to obtain, in a stable situation (display synchronizer; '882; col. 17, ln. 50-58, col. 18, ln. 1-10), the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period ('882; col. 17, ln. 12-20; the pointers) and does not teach a ratio of two between the display frame rate and the source frame rate. Schiefer, however, teaches a ratio of four between the display frame rate and the source frame rate ("882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) and Schiefer does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as may be desired and is shown in '882; col. 21, ln. 15-20. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

In regard to claim 2, Schiefer teaches a display system comprising: a video source for generating images comprising source data (input video; '882; fig. 1 & 2; col. 10, ln. 14-26) and source frame (vertical) synchronization instants (IPVSYNC), having a source frame rate, means for storing the source data in a frame memory (memory, '882; fig. 3; col. 11, ln. 51-58) under control of a first address pointer (write counter) having a start address being determined by the source frame synchronization instants (IPVSYNC) ('882; col. 13, ln. 13-39); means for reading during a read period display data from the memory under control of a second address pointer (read counter) having a start address being determined by display frame synchronization instants

(DVSYNC) having a display frame rate ('882; col. 14, ln. 5-35), means for displaying the display data on a matrix display ('882; fig. 2) and means for controlling the source frame rate or the display frame rate to obtain, in a stable situation (display synchronizer; '882; col. 17, ln. 50-58, col. 18, ln. 1-10), the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period ('882; col. 17, ln. 12-20) and does not teach a ratio of two between the display frame rate and the source frame rate. Schiefer, however, teaches a ratio of four between the display frame rate and the source frame rate ("882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) and Schiefer does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as may be desired and is shown in '882; col. 21, ln. 15-20. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when the input image data rate is 1/2 half the screen refresh rate of the video display.

Regarding claim 3, Schiefer further teaches a display system wherein the means for controlling comprise: means for comparing the source frame synchronization instants (IPVSYNC) and the display synchronization instants (DVSYNC) or signals related thereto ('882; fig. 13; col. 21, ln. 15-34), and means for adapting the source frame rate or the display frame rate in response to the comparing to obtain the second pointer always lagging ("882; fig. 13, DTGRUN signal) the first pointer during the read period in times or the other way around ('882; fig. 13; col. 21, ln. 15-34).

Regarding claim 4, Schiefer further teaches a display system wherein the means for controlling comprise: means for determining the offset in time between one of the source frame synchronization instants (IPVSYNC) and one of the display frame synchronization instants (DVSYNC) succeeding each other("882; col. 21, ln. 34-46), and means for adapting the source frame rate or the display frame rate to obtain a substantially identical source frame rate and display frame rate ('882; col. 21, ln. 34-46); and a predetermined fixed value of the offset in time ('882; fig. 13, DTGRUN signal).

Regarding claim 5, Schiefer teaches a display system as claimed in claim 4 but does not teach wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data. Schiefer teaches pre-filling the buffer memory to ensure that the display output can provide continuous horizontal active data regions ('882; col. 14, ln. 5-35). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data for the benefit of maintaining the optimum buffer fill to allow the most overrun and under run protection to handle short term variations is input video and output display timing that may occur in any system operating over a range of environmental conditions such a temperature, voltage, etc.

In regard to claim 6, Schiefer further teaches a display system as claimed in claim 2, wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), and means for generating the display frame synchronization instants using the clock signal (DVSYNC; '882, fig. 10); and wherein the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal ('882; col. 15, ln. 29-37; col. 20, ln. 9-14).

Regarding claim 7 (Previously Presented), Schiefer further teaches a display system wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), means for generating line instants indicating a start of the lines of the display data using the clock signal (DHSYNC; '882; fig. 9), the line instants (DHSYNC) determining line periods, and means for generating the display frame synchronization instants (DVSYNC) using the line instants (DHSYNC) ('882; col. 21, ln. 23-28), and wherein the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods ('882; col. 15, ln. 29-37; col. 20, ln. 9-14).
In regard to claim 8 (Previously Presented), Schiefer further teaches a display system wherein the means for displaying the display data further comprise: means for generating a clock signal (DCLK; '882; fig.7), means for generating line instants indicating a start of the lines of the display data by counting the clock signal (DHSYNC; '882; fig. 9), the line instants determining line periods, and means for generating the display frame synchronization instants (DVSYNC) using the line instants ('882; col. 21, ln. 23-28), and wherein the means for controlling the

display frame rate comprise means for adapting the line periods by varying a number of clock pulses of the clock signal to be counted ('882; col. 22, ln. 9-35).

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefer et al. (European Patent Application Publication EP 0 875 882 A2, hereafter, '882) as applied to claims 1-8 above, and further in view of Chen et al. (U. S. Patent Application 2003/0164897 A1, hereafter '897).

Regarding claim 9, Schiefer teaches a display system method as claimed in claim 2 but does not teach wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for read period and an idle period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and wherein during the idle period no display data is read from the memory and wherein the means for controlling the display frame rate comprises means for varying the idle time. Chen, working in the same field of endeavor, however, teaches wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for read period and an idle period (current line delay), wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer (output x & y counters), and wherein during the idle period (current line delay) no display data is read from the memory (outputs blank lines) and wherein the means for controlling the display frame rate comprises means for varying the idle time ('897; fig. 7; ¶ 0124) for the benefit of synchronizing video image input and display image output frame rates

without adjusting either the input or output video clock frequencies thereby simplifying overall clock circuit design and lowering cost. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Schiefer and Chen to produce a method that controls the output video idle period to synchronize the video output frame rate to the video input frame rate with the benefit of not adjusting either of the input or output video clock frequencies thus simplifying overall clock circuit design and lowering cost.

In regard to claim 10, Chen further teaches wherein the means for controlling comprise: means for determining the offset in time, and means for adapting the display frame rate to obtain a display frame rate being substantially identical to two times the source frame rate and to obtain a predetermined fixed offset in time, by having (i) the second pointer (output x & y counters) pointing to a first source video line of an already stored source video frame at an instant preceding the instant the first pointer (input x & y counters) is pointing to a first source video line a next source video frame to read the first source video line before the first source video line of the next source video frame is stored, and (ii) the second pointer (output x & y counters) pointing to a last source video line of the next source video frame at an instant later than an instant the first pointer (input x & y counters) is pointing to the last source video line of the next source video frame to read the last source video line of the next source video frame after it has been stored ('897; fig. 8-9, ¶ 0127-0128).

Regarding claim 11, Chen further teaches a display system wherein a display frame period has a duration being an inverse of the display frame rate and comprises the read period and an idle

period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer (output x & y counters), and wherein during the idle period no display data is read from the memory (outputs blank lines) and wherein the means for controlling comprise: means for setting a free running display frame rate to a value lower than the value of the source display frame rate wherein a duration of the read period is shorter than a source frame period ('897; ¶ 0115), and means for restarting the display frame periods in response to received source (input vertical) synchronization instants ('897; fig. 3, ¶ 0117).

(10) Response to Argument

The Applicant's remarks begin with:

Rejection of Claims 1-8 Under 35 U.S.C. § 103

The Final Office Action dated June 11, 2009, rejects claims 1-8 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer. Applicant respectfully traverses this rejection.

Claims 1 & 2

Independent claim 1 recites, in part, "A display method comprising . . . controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate (emphasis added).Independent claim 2 contains similar recitations.

As described in the specification in paragraph [0009], this subject matter relates to the use of a controller to control both the read and write address pointers in the memory that uses a single circular buffer in order to prevent video tearing. When the source and display frame rates are not equal, the controller adjusts both the frame rates and the address pointers so that, during the read period, one pointer does not cross the other, thus preventing tearing. *See qf* [0015], [0063]. Such adjustments have advantages, such as lowering the required source frame rate, lower power consumption, and reduce flickering. *See ~f* [0063]. This is highlighted by three features: (1) a time offset between the two address pointers, (2) a fixed polarity of the pointers during the read period, and (3) a constant ratio between the display frame rate and the source frame rate (here, the ratio is equal to 2). *See* ¶ [0054].

In contrast, Schiefer fails to disclose, teach, or suggest "controlling means for controlling the source frame rate or the display frame rate to obtain the address pointers, where the pointers start with a time offset, there is a fixed polarity between the pointers, and there is a ratio of two between the display and source frame rates," as recited in claim 1 and similarly recited in claim 2. Schiefer discloses a timing generator for format conversion of video. *See Abstract.* This system reformats video by *synchronizing* the output and input frame rates, using a memory buffer in case of errors to ensure a smooth display. The memory write controller controls write operations sequentially in a circular buffer sequence. *See col. 13, lns. 34-39.* The data path, once full, is then controlled by a timing controller.

The Examiner respectfully disagrees with the above in that the memory buffer of the Schiefer reference is not used in case of errors; it is used to insure that there is enough data available ahead of starting a display frame to **prevent any tearing or like errors** in the display process. This buffer is equivalent to the circular buffer of the instant application which is also preloaded with data before the display is released to read from the buffer.

The Applicant continues writing:

In section 19 on page 12, the Office Action states that Schiefer "points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given" (emphasis in original). As this timing diagram of the *clock rates* indicates, Schiefer substantially differs in operation from the recited subject matter.

The recited subject matter recites a ratio of two between the display frame rate and the source frame rate~ as the single circular buffer allows *at maximum, a* ratio of 2 (1:2 or 2:1) between the respective frame rates to function properly without any video tearing. *See e.g., Figs. 5A-5E, ¶ [0061]-[0063].* The ratio of 4:1 disclosed by Scheifer and cited by the Examiner as the ratio between the respective address pointers in the singular buffer would guarantee video tearing, as one pointer with a rate four times faster than the other would always overtake the other pointer during at some point in the circular buffer and would do so multiple times during a single traversal of the slower pointer through the circular buffer.

Furthermore, Schiefer discloses a system that scales and deinterlaces the input video and *matches the frame rate* of the input video with that of the output. The large ratio between input and output *clock rates* ("DCLK = 4*IPCLK", *see Fig. 11)* disclosed by Schiefer and cited by the Examiner **does not** relate the ratio between the *input and output frame rates* recited by the above subject matter. Rather, the 4:1 ratio discussed in the Schiefer specification relates to the system horizontally and vertically upscaling,,an input image by a factor of 2 for an output video, while maintaining the locked, similar frame rate through the control of the respective *line rates, (see col. 21, lns. 15-33* (discussing display line rate as a fractional multiple of the input video main clock)). These line rates differ due to the respective number of pixels per

line in the input and output images. *See, col. 21, lns. 34-46* (discussing means to force frame locking so the resulting display frame period is similar to the input video frame period.)

A person of ordinary skill in the art, therefore, would not refer to Schiefer, which discloses a solution for scaling a video image using a 4:1 clock ratio for line rates, to create the recited subject matter, which has a maximum working limit of 2:1 between frame rates, as Schiefer's disclosure would make the recited subject matter unusable. The Examiner has used impermissible hindsight to conclude that a person of ordinary skill in the art would refer to a device that explicitly discloses an unworkable range between variables in order to create the recited subject matter. Therefore, Schiefer does not disclose, teach, or suggest, "controlling the source frame rate or display frame rate to obtain . . . a ratio of two between the source frame rate and the display frame rate," as recited in independent claim 1 and similarly recited in independent claim 2.

The Examiner respectfully disagrees with the Applicant's analysis above. To begin, the abstract of Schiefer provides a good overall view of the Schiefer invention which covers the functionality of the instant application but does not get into the actual clock rates as it is only an abstract.

"This invention is directed to a method and apparatus for producing video signal timing for a display device that has a display format different from the input video format. It also provides a method and apparatus for producing video signal timing in cases where the input video line rate and display output line rates are not the same. Furthermore, a method and apparatus are provided for synchronizing the display output line rate to the input rate so that the source video line input rate can sustain the rate at which the input lines are processed to generate display video lines using a minimum amount of memory buffer for a variety of display processing methods. Another aspect of the present invention provides a method and apparatus for synchronizing display output timing to input video timing such that both are locked in terms of frame rate, but skewed in terms of frame phase, in order to accommodate latency incurred by processing of source video data to generate the display video data. A method and apparatus are also contemplated by this invention for adjusting the skew between the input source video frame timing and the display output video from timing to accommodate latency for various types of display processing such as, but not limited to, scaling, video format conversion, and filtering operations"

Note that if the input line rates and output line rates as stated in the abstract above, differ, then the frame rates are likely to differ, assuming that the total line count in the input and the output formats are similar. With this background established, please refer to figure 4 of Schiefer, which is a block diagram showing a memory write controller, a memory for buffering display data and

a display timing controller for controlling the reading of display data out of the buffer memory and passing it on to the display processor that outputs to the actual display device.

Schiefer teaches a write pointer into the buffer memory (actually two, if needed, so that interlaced formats can be easily changed to a progressive format; ('882; col. 12, ln. 35-52) and a read pointer to allow reading data out of the buffer memory for display. As the Applicant noted, Shafer starts writing into the buffer memory and waits until the buffer is half full **thus providing the fixed polarity offset between the pointers as required by claims 1 and 2** and the last cite in claims 1 and 2 ("882; fig. 11-15, DCLK = 2*IPCLK, col. 21, ln. 15-20) points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given, thus is a factor of 2 times greater the teachings of the last element or limitation in claims 1 and 2 that states that the rates are related by a factor of two. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when one is given the design criteria as stated in the specification of the instant application of the input image data rate being 1/2 half the screen refresh rate of the video display (¶ 0022 of the US 2007/0159490, the Patent Application Publication of the instant application). Obviously, if the embodiment example were one where the input is 1/4 the output rate, the example given in the Schiefer reference would match exactly. This analysis is not hindsight reconstruction; it is engineering design procedure that would be driven by the actual equipment/product performance requirements specification. Schiefer's design covers variable ratios and is not locked into one specific ratio as presented in the instant application.

Schiefer does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as stated in col. 21, ln. 15-20 so that it is not constrained to multiples of the horizontal line or image frame/field rates. The example given by Schiefer is obviously one where the input and output rates are in the ratio of 1 to 4.

The Applicant continues writing:

In addition, while Schiefer does disclose a half-line offset, Schiefer discloses a half-line offset "to maintain a constant period between lock events" with the source and output *having the same frame rates,* with the offset time used to minimize timing errors. *See col. 17, lns. 17-20.* This motivation is different from the recited subject matter, which uses a half-line offset to allow the system to properly *support* differing frame rates, to a maximum of a 2:1 ratio. Schiefer, therefore, does not disclose, teach, or suggest an offset to support a non-identical ratio between input and output frame rates, nor does Schiefer disclose, teach, or suggest any support of a non-identical ratio of two between the display frame rate and the source frame rate. See, e.g., col. 21, lns. 34-46. As such, Schiefer fails to disclose, teach, or suggest to a person of ordinary skill in the art all the elements recited in claims 1 and 2. Schiefer therefore does not render claims 1 and 2 obvious.

The Examiner respectfully disagrees with the Applicant's analysis above. Referring to figure 4 of Schiefer, there is provided a memory write controller, a memory for buffering display data and a display timing controller for controlling the reading of display data out of the buffer memory and passing it on to the display processor that outputs to the actual display device. Schiefer teaches a write pointer into the buffer memory (actually two, if needed, so that interlaced formats can be easily changed to progressive format; col 12, ln. 35-52) and a read pointer to allow reading data out of the buffer memory. The ½ line offset noted above is for the case **locking of an interlaced format** (to provide the stable condition of the instant application) and is not intended to show only ½ line buffering and, as previously stated, Shafer starts writing

into the image data buffer memory and waits until the buffer is half full **thus providing the fixed polarity offset between the pointers as required by claims 1 and 2** and the last cite in claims 1 and 2 ("882; fig. 11-15, DCLK = 4*IPCLK, col. 21, ln. 15-20) points to the detailed timing diagrams of the data buffering section of the invention where it is shown that the **output write clock is running at rate of four times the input clock rate** in the example given, thus is a factor of 2 times greater the teachings of the last element or limitation in claims 1 and 2 that states that the rates are related by a factor of two. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the design choice of a ratio of two between the display frame rate and the source frame rate for the benefit of having a stable video display when one is given the design criteria as stated in the specification of the instant application of the input image data rate being 1/2 half the screen refresh rate of the video display (¶ 0022 of the US 2007/0159490, the Patent Application Publication of the instant application). Obviously, if the embodiment example were one where the input is 1/4 the output rate, the example given in the Schiefer reference would match exactly. This analysis is not hindsight reconstruction; it is engineering design procedure that would be driven by the actual equipment/product performance requirements specification. Schiefer's design covers variable ratios and is not locked into one specific ratio as presented in the instant application. Schiefer does not limit the ratio to a factor of 4, as it can be a fractional multiple of the input video main clock (pixel rate) as stated in col. 21, ln. 15-20 so that it is not constrained to multiples of the horizontal line or image frame/field rates. The example given by Schiefer is obviously one where the input and output rates are in the ratio of 1 to 4.

The Applicant's remarks continue:

Claims 3-8

Claims 3-8 depend on claim 2 and are therefore also allowable for at least the reasons detailed above in connection with independent claims 1 and 2, as well as for the separately patentable subject matter recited therein.

The Examiner respectfully replies that claims 3-8 are rejected as being dependent upon independent claim 2 which is rejected as shown in section 9 of this document and as argued above. Additionally, the additional limitations that they add are rejected as shown in the rejection of each specific claim as shown in section 9 of this document.

The Applicant's remarks continue:

Rejection of Claims 9-11 Under 35 U.S.C. § 103

The Final Office Action dated June 11, 2009, rejects claims 9-11 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer in view of Chen. Applicant respectfully traverses these rejections.

Claims 9-11 depend from independent claim 2. Chen discloses a system to prevent buffer over- or under-flow, with the input and output rates being equal. See Abstract. Chen also discloses a display frame period being the inverse of the display frame rate and controlling the display frame rate by adjusting the idle time (time between read periods). Chen therefore fails to overcome the deficiencies of Schiefer described above in connection with independent claim 2.

Claims 9-11 are therefore patentable for at least the reasons stated above in connection with claim 2, as well as for the separately patentable subject matter recited therein.

The Examiner respectfully replies that Chen was not used in the rejections of claims 1 and 2. Chen teaches the additional elements of claims 9-11 and the Examiner's remarks with respect to claim 2 upon which these claims depend have been addressed above in the arguments directed to claims 1 and 2, thus, restating the issues with claim 2 as applying to claim 9-11 is without merit.

Claims 9-11 are properly rejected as to the additional features they add and are rejected by the Examiner as shown in section 9 above. This concludes the Applicant's remarks and the Examiner's response to the same.

The Examiner's final remarks are to point out that this application claims priority from application number 04100283.3, filed with the European Patent Office on 28 January 2004, a copy of which was submitted as part of the IDS provided with the initial US Patent Application. Also part of this IDS submission is the International Search Report issued on 12 May 2005 indicating the European Patent Publication, EP 0 875 882 A, the primary reference used by the Examiner in the instant application, is a category X reference applicable to all 12 claims of that application.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Edward Martello/

Conferees:

/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628

/Kee M Tung/

Supervisory Patent Examiner, Art Unit 2628